

U.S. Serial No. 10/750,489

Response to the Office action of July 8, 2005

This listing of claims will replace all prior versions, and listings, of claims in the application:

**The Status of the Claims**

1. (Currently Amended) A method of fabricating an MIM capacitor of high capacitance in a semiconductor device, the method comprising:  
depositing an interlayer dielectric film on a metal line;  
etching the interlayer dielectric film to form an MIM capacitor forming region;  
sequentially depositing a lower electrode layer, an insulator layer and an upper electrode layer on the interlayer dielectric film; and  
etching the lower electrode layer, the insulator layer and the upper electrode layer to form an MIM capacitor[.], wherein a capacitance of the MIM capacitor is determined by controlling a thickness of the interlayer dielectric film.
2. (Canceled)
3. (Original) A method as defined by claim 1, wherein the interlayer dielectric film is made of USG or TEOS.
4. (Original) A method as defined by claim 1, wherein the lower electrode layer is made of Ti, W or TiN.
5. (Original) A method as defined by claim 1, wherein the insulator layer is made of TaO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub> or SiN.
6. (Original) A method as defined by claim 1, wherein the upper electrode layer is made of Ru, Pt or TiN.
7. A method of fabricating an MIM capacitor of high capacitance in a semiconductor device, the method comprising:  
depositing an interlayer dielectric film on a metal line;  
planarizing the interlayer dielectric film;  
etching the interlayer dielectric film to form an MIM capacitor forming region;  
sequentially depositing a lower electrode layer, an insulator layer and an upper electrode layer on the interlayer dielectric film; and  
planarizing the lower electrode layer, the insulator layer and the upper electrode layer

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to form an MIM capacitor[.], wherein a capacitance of the MIM capacitor is determined by controlling a thickness of the interlayer dielectric film.

8. (Canceled)

9. (Original) A method as defined by claim 7, wherein the interlayer dielectric film is planarized by a chemical mechanical polishing (CMP) process.

10. (Original) A method as defined by claim 7, wherein the interlayer dielectric film is planarized by an etch-back process.

11. (Original) A method as defined by claim 7, wherein the lower electrode layer is made of any one of Ti, W or TiN.

12. (Original) A method as defined by claim 7, wherein the insulator layer is made of any one of TaO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub> or SiN.

13. (Original) A method as defined by claim 7, wherein the upper electrode layer is made of any one of Ru, Pt or TiN.

14. (Original) A method as defined by claim 7, wherein the lower electrode layer, the insulator layer and the upper electrode layer are planarized by a chemical mechanical polishing (CMP) process.

15. (Original) A method as defined by claim 7, wherein the lower electrode layer, the insulator layer and the upper electrode layer are planarized by an etch-back process.